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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,286	02/12/2004	Makoto Onozawa	122.1581	3508

21171 7590 11/16/2005

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EXAMINER	
AL NAZER, LEITH A	

ART UNIT	PAPER NUMBER
2821	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/776,286	ONOZAWA ET AL.	
	Examiner	Art Unit	
	Leith A. Al-Nazer	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *36-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *36-42,44 and 47-50* is/are rejected.

7)☒ Claim(s) *43,45 and 46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2004 and 24 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *16 September 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 39 is objected to because of the following informalities:

Claim 39 recites "a power supply terminal" in both lines 1-2 and again in line 3. The claim should be amended to recite a first power terminal and a second power terminal.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 36-42, 44, and 47-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,426,594 to Ito in view of International Application WO 02/095914 A2 to Stanley.

With respect to claim 36, Ito teaches a plasma display apparatus, comprising: a plurality of X electrodes (figure 5), a plurality of Y electrodes arranged adjacently to the plurality of X electrodes by turns and each causing a discharge to occur between the neighboring X and Y electrodes (figure 5), an X electrode drive circuit (51) for applying a discharge voltage to the plurality of X electrodes, and a Y electrode drive circuit (52) for applying a discharge voltage to the plurality of Y electrodes; and the plurality of drive systems being provided within an IC formed on a common semiconductor chip (column 3, lines 14-36). Claim 36 requires at least one of the X electrode drive circuit and the Y electrode drive circuit comprising a first switch supplying a high level voltage to the plurality of X electrodes or the plurality of Y electrodes, a second switch supplying a low level voltage to the plurality of X electrodes or the plurality of Y electrodes, and a pre-drive circuit driving the first switch and the second switch; the pre-drive circuit comprising a plurality of drive systems each having an input amplifier circuit amplifying an input voltage, input to an input voltage terminal, a high level shift circuit shifting a level of a signal output from the input amplifier circuit and an output amplifier circuit amplifying a shift signal output from the high level shift circuit, wherein each drive system has a common constitution. Stanley teaches such a configuration (figures 2-5). Specifically, Stanley teaches at least one of the X electrode drive circuit and the Y electrode drive circuit comprising a first switch (7) supplying a high level voltage to the

plurality of X electrodes or the plurality of Y electrodes, a second switch (9) supplying a low level voltage to the plurality of X electrodes or the plurality of Y electrodes, and a pre-drive circuit (8 and 8') driving the first switch and the second switch; the pre-drive circuit comprising a plurality of drive systems each having an input amplifier circuit (56 and 58 in figure 5) amplifying an input voltage, input to an input voltage terminal, a high level shift circuit (10, 14, 18, 20, 25-28, and 30) shifting a level of a signal output from the input amplifier circuit and an output amplifier circuit (32) amplifying a shift signal output from the high level shift circuit, wherein each drive system has a common constitution (8 and 8' in figure 2). At the time of the invention, it would have been obvious to one having ordinary skill in the art to provide the display system of Ito with the driving circuit configuration of Stanley. The motivation for doing so would have been to provide the system of Ito with a driver circuit that minimizes the effects of high voltage, hard switching (see page 2, lines 21-26 of Stanley).

With respect to claim 37, Stanley teaches each drive system including a low level shift circuit shifting a level of a signal, output from the input amplifier circuit, to a signal referred to a negative reference voltage, and the high level shift circuit shifts the level of the signal output from the low level shift circuit (figures 2-5).

With respect to claim 38, Stanley teaches each drive system including a waveform processing circuit (10) processing a waveform of the signal output from the low level shift circuit, the high level shift circuit shifts the level of the signal output from the waveform processing circuit, and the waveform processing circuit being connected to a negative reference voltage input terminal, to which the negative voltage is input,

and a negative supply voltage input terminal, to which a negative supply voltage, having a predetermined voltage referred to the negative reference voltage, is input (figures 2-5).

With respect to claim 39, Stanley teaches a power supply terminal (20), supplying a drive power supply of the input amplifier circuits of the plurality of drive systems, and a power supply terminal (28), supplying a drive power supply of the output amplifier circuits of the plurality of drive systems and the negative supply voltage input terminal, being separately provided (figures 2-5).

With respect to claim 40, Stanley teaches the waveform processing circuit being a Schmitt trigger circuit (10).

With respect to claim 41, Stanley teaches the waveform processing circuit having an integrating circuit to eliminate noise (10).

With respect to claim 42, Stanley teaches two of the drive systems of the plurality of drive systems being paired (8 and 8' in figures 2-5), and each pair including a simultaneous ON avoiding circuit to maintain an output of one of the two drive systems of the pair to be inactive when an output of the other of the two drive systems of the pair is active (70 in figure 5).

With respect to claim 44, Stanley teaches a previous stage or a subsequent stage of the plurality of drive systems of the pre-drive circuit further comprising a delay time adjusting circuit (70 in figure 5) to adjust an input time and output time of a signal.

With respect to claim 47, Stanley teaches the high level voltage being a supply voltage and the low level voltage being a ground voltage (figures 2-5).

With respect to claim 48, Stanley teaches the high level voltage being a positive voltage and the low level voltage being a negative voltage having an absolute value which is the same as that of the high level voltage (figures 2-5).

With respect to claim 49, Stanley teaches a previous stage of a plurality of input voltage terminals of the pre-drive circuit comprising an input level shift circuit to convert a level of an input signal referred to a ground voltage into one referred to the low level voltage (70 in figure 5).

With respect to claim 50, Stanley teaches a reset pulse (26) being supplied to at least one of the X and Y electrodes, and a low voltage, which is applied to a terminal of the second switch, being increased when the reset pulse is supplied.

Response to Arguments

5. Applicant's arguments, see pages 8 and 9 of the amendment filed on 24 October 2005, with respect to the rejection(s) of claim(s) 1-35 under 35 USC 102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection for currently pending claims 36-50 is made in view of newly cited prior art U.S. Patent No. 6,426,594 to Ito in view of International Application No. WO 02/095914 to Stanley. In the amendment filed on 24 October 2005, Applicant preliminarily argued that the newly cited prior art to Stanley "has no description that the gate drivers 8 and 8' are provided within an IC formed on a common semiconductor chip". Examiner agrees. However, the benefits of

incorporating an IC into a single chip configuration is well known in the art, as is evidenced by Ito (column 3, lines 14-36).

Allowable Subject Matter

6. Claims 43, 45, and 46 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest one or more of the limitations found in dependent claim 43. Specifically, the prior art of record fails to teach or suggest the combination of a third switch supplying a high level voltage to the plurality of X electrodes or the plurality of Y electrodes via a first coil, and a fourth switch supplying a low level voltage to the plurality of X electrodes or the plurality of Y electrodes via a second coil.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leith A. Al-Nazer whose telephone number is 571-272-1938. The examiner can normally be reached on Monday-Friday, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on 571-272-1834. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LA

Shih-Chao Chen 11/12/05

SHIH-CHAO CHEN
PRIMARY EXAMINER